ABSTRACT

A phase locked loop (PLL) circuit including a phase comparator 2 that compares a phase of a reference clock signal with that of a comparison clock signal to produce a phase comparison signal having three-level outputs of a high voltage (H) level, a low voltage (L) level, and a reference level, and outputs an H or L level signal for duration corresponding to a detected phase difference or outputs a reference level signal when there is no phase difference detected; a level shifter 3 that serves to hold the rectangular waveform of the phase comparison signal from the phase comparator 2; a voltage controlled oscillator (VCO) 4 that advances the phase upon receipt of the H level signal and delay the phase upon receipt of the L level signal; and a frequency divider 5 that divides a frequency of an oscillation clock from the VCO 4 to produce a comparison clock signal.